REMARKS

In the Office Action mailed January 11, 2005, claims 1-4, 6-27 are rejected under 35 USC §102(e) as being anticipated by Nadeau-Dostie et al., (US Patent 6,829,730, hereinafter "Nadeau-Dostie"). Claim 5 is rejected under 35 USC §103(a) as being obvious in view of Nadeau-Dostie.

In response to the rejections, Applicant respectfully submits that the claims as pending clearly distinguish over Nadeau-Dostie, and request reconsideration of the claims. Nadeau-Dostie is directed to a circuit having multiple test access ports (TAPS). A Master TAP functions as the circuit test bus for controlling data transfer operations with the remaining secondary TAPs in the circuit. The secondary TAPs are connected between the circuit TDI and circuit TDO in one or more TAP groups. A selection code stored in the Master TAP instruction register is loaded with each instruction. The selection code specifies the next TAP group which will be involved in a data transfer operation. A TDO selector responds to the selection code by connecting the group TDO of the specified group to the circuit TDO. To simplify instruction loading operations, the length of the TDI-TDO path through each TAP group is the same for all groups, including the Master TAP group. A "padding register" may be added to make all of the instruction registers of the TAP groups equal. (Col. 2, lines 36-63). As shown in Fig. 3, the padding register comprises the necessary number of elements of the Master TAP.

However, Nadeau-Dostie teaches away from Applicant's claims by teaching a master tap having a fixed length, and embedded taps which are coupled to padding registers so that all of the TAPs have the same fixed length. That is, the length of the Master TAP is fixed, and equal to the length of the longest group of embedded TAPs. The lengths of groups of embedded TAPs are provided with "padding registers" to make them the same length. As will be described below, each of the independent claims includes limitations which clearly distinguish over Nadeau-Dostie.

Independent Claim 1

Independent claim 1 is directed to a method for flexibly nesting JTAG TAP controllers for IP cores in a FPGA-based system-on-chip (SoC). Claim 1 includes steps of:

> selecting at least one available bit from a selectable bit register of a host JTAG TAP controller, said selectable bit register having a plurality of available bits; and
>
> extending an apparent length of an instruction register of said host JTAG TAP controller by using said at least one available bit from said selectable bit register.

Nadeau-Dostie fails to disclose a "selectable bit register" of a host JTAG TAP controller which extends "the apparent length of an instruction register of the host JTAG TAP controller." Rather, the only instruction register of the Master TAP 100(i.e. instruction register 125) is a fixed bit register. As shown in Fig. 3, instruction register 125 always has eight elements. More importantly, instruction register 125 (of the Master TAP 100) is not used to extend the length "of an instruction register of the host JTAG TAP controller." While some TAP groups may have a different length, the input to the tap group is coupled to a predetermined number of elements of the instruction register 125 of the Master TAP 100. However, using some of the elements of instruction register 125 to make the instruction registers of the embedded taps have an equal length does not extend the apparent length of an instruction register "of the host JTAG TAP controller." That is, the instruction register 125 itself is not selectable as claimed by Applicant. Accordingly, Applicant submits that language of claim 1 as pending clearly distinguishes over Nadeau-Dostie, and that claim 1 and dependent claims 2-6 are allowable over Nadeau-Dostie.

Independent Claim 7

Independent claim 7 is directed to a method for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. The method of claim 7 comprises a step of "selecting an apparent register size based upon a number of IP cores implemented in the FPGA-based SoC." In contrast to claim 7, Nadeau-Dostie selects

a register size based upon the largest register for any TAP or group of TAPS coupled in the TDI-TDO path of Master TAP 100. Accordingly, Applicant submits that claim 7 as pending clearly distinguishes over Nadeau-Dostie, and that claim 7 and dependent claims 8-10 are allowable over Nadeau-Dostie.

Independent Claim 11

Claim 11 is directed to a system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. The system of claim 11 comprises:

> a selectable bit register in a host JTAG TAP controller comprising at least one available bit; and
>
> a selector for selecting said at least one available bit, said selector extending an apparent length of an instruction register of said host JTAG TAP controller by using said selected at least one available bit from said selectable bit register.

In addition to failing to disclose a "selectable bit register" in a Host JTAG TAP controller as set forth above with respect to claim 1, Nadeau-Dostie clearly fails to disclose or suggest "a selector for selecting said at least one available bit, said selector extending an apparent length of an instruction register of said host." It is suggested in the Office Action that the selector of claim 11 is disclosed by multiplexer 132 of Nadeau-Dostie. However, embedded TAP groups 102, 104 and 106 of Nadeau-Dostie are not a part of the Master TAP 100. More importantly, multiplexer 132 of Nadeau-Dostie is not a selector for extending the apparent length of the instruction register. Rather, multiplexer 132 is controlled by the Shift-IR control signal to determine the source of the data loaded into a TAP group. When an instruction is loaded into an instruction register, Shift-IR is active (Logic 1), which connects input 1 of each of multiplexers 132 and 134 to their respective group TDI input. Conversely, when data is being loaded into a test data register, Shift-IR is inactive (logic 0), which connects input 0 of each of multiplexers 132 and 134 to the group TDI input. (Col. 10, line 57 to Col. 11, line 1). Unlike the selectable bit register of claim 11, the instruction register 125 of Nadeau-Dostie is a fixed length register which is determined by the

largest register for any TAP or group of TAPS coupled in the TDI-TDO path of Master TAP 100. Further, multiplexer 132 merely selects whether embedded tap groups 102, 104 and 106 function as instruction registers or data registers. Accordingly, Applicant submits that claim 11 and dependent claims 12 and 13 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

Independent Claim 14

Independent claim 14 is directed to a system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. The system comprises "an instruction register size select signal enabling the selection of an apparent register size to accommodate a variable number IP cores." It is suggested in the Office Action that the "instruction register size select signal" of claim 14 is also disclosed by multiplexer 132 of Nadeau-Dostie. However, as set forth above with respect to claim 11, multiplexer 132 of Nadeau-Dostie is not a selector for enabling the selection of an apparent register size. Rather, the select signal for multiplexers 132 and 134 merely select whether embedded TAP groups 102, 104 and 106 function as instruction registers or data registers. Applicant respectfully submits that Nadeau-Dostie fails to disclose an instruction register size select signal as claimed by Applicant. Accordingly, Applicant submits that claim 14 and independent claims 15-17 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

Independent Claim 18

Independent claim 18 is directed to a method for ensuring an information register length for nested JTAG TAP controllers for IP cores remains the same "before and after a configuration of an FPGA" in an FPGA-based system-on-chip (SoC). The method comprises step of:

> forming instruction registers for the IP cores that are in series with the instruction registers of the FPGA of the SoC;

> forming connections between FPGA JTAG logic of the FPGA and IP Core JTAG logic of the IP core using a programmable interconnect; and
>
> emulating an instruction register of the IP core prior to configuration of the FPGA using a shift register of the same length as the instruction register of the IP core.

Applicant respectfully submits that Nadeau-Dostie fails to disclose or suggest any of the steps of claim 18. There is no mention is the Office Action of the disclosure of an FPGA as claimed by Applicant. More specifically, Nadeau-Dostie fails to disclose or suggest (i) forming connections between FPGA JTAG logic of the FPGA and IP Core JTAG logic of the IP core using a programmable interconnect, or (ii) emulating an instruction register of the IP core prior to configuration of the FPGA. Accordingly, Applicant respectfully submits that independent claim 18 and dependent claims 19-20 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

Independent Claim 21

Independent claim 21 is directed to a system for performing boundary scan functions on a plurality of IP cores. The system comprises:

> an FPGA-based system-on-chip (SoC) comprising a plurality of IP cores each including a first JTAG TAP controller; and
>
> a host JTAG TAP controller coupled to each of the first JTAG TAP controllers, said host JTAG TAP controller comprising a selectable bit register enabling the selection of an apparent register size to accommodate a variable number of IP cores.

In response to the rejection, Applicant also submits that Nadeau-Dostie fails to disclose or suggest an FPGA-based system-on-chip (SoC) comprising a plurality of IP cores each including a first JTAG TAP controller. Nadeau-Dostie also fails to disclose or suggest a host JTAG TAP controller comprising "a selectable bit register enabling the selection of an apparent register size to accommodate a variable number of IP

cores," for the same reasons set forth above. Accordingly, Applicant respectfully submits that claim 21 and dependent claims 22-27 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 7, 2005.

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